What is claimed is:

1. A capacitor formed on a semiconductor substrate, the capacitor comprising:

a first electrode of a first metal layer;

a second electrode of a second metal layer that is closer to the substrate than the first metal layer;

a dielectric material intermediate the first and second electrodes; and

a wire coupled to a bottom surface of the first electrode

2. The capacitor of claim 1 wherein the wire is formed of a third metal layer that is closer to the substrate than the second metal layer.

3. The capacitor of claim 1 wherein the wire is formed of the second metal layer.

4. The capacitor of claim 1 wherein the wire is coupled to the first electrode through a contact hole.

5. The capacitor of claim 4 wherein the contact hole comprises a plurality of separate contact holes.

6. The capacitor of claim 1 wherein the wire has a planarized top surface.

7. The capacitor of claim 6 wherein the wire comprises a damascene layer.

8. A metal-insulator-metal capacitor, comprising:

a wire layer formed in a first metal layer, the wire layer including a first electrode contacting line;

a bottom electrode formed in a second metal layer;

a top electrode formed in a third metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode; and

a contact formed between the electrode contacting line and a bottom side of the top electrode.

9. The capacitor of claim 8 wherein the top electrode couples to the first electrode contacting line through a contact hole in the dielectric layer.

10. The capacitor of claim 9 wherein the contact hole comprises a plurality of separate holes.

11. The capacitor of claim 8, wherein the wire layer comprises a second electrode contacting line, and wherein the second electrode contacting line is coupled to a bottom surface of the bottom electrode.

12. The capacitor of claim 11, wherein a portion of the bottom surface of the bottom electrode directly contacts a top surface of the second electrode contacting line and not through a contact hole.

13. The capacitor of claim 11 wherein the bottom electrode couples to the second electrode contacting line through a contact hole in an insulation layer.

14. The capacitor of claim 11 wherein the first and second electrode contacting lines each have a planarized top surface.

15. The capacitor of claim 14 wherein the first and second contacting lines are planarized by a damascene process.

16. The capacitor of claim 14 wherein the first and second contacting lines are planarized by a CMP process performed on an interlayer dielectric layer.

17. The capacitor of claim 11 wherein a top surface of the first and second contacting lines are formed in a process other than planarization.

18. The capacitor of claim 8, further comprising a second contact located on a top side of the bottom electrode.

19. The capacitor of claim 18, wherein the second contact extends away from the substrate farther than the third metal layer.

20. A metal-insulator-metal capacitor, comprising:

a first metal layer including a bottom electrode and an electrode contacting line;

a top electrode formed in a second metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode; and

a contact formed between the electrode contacting line and a bottom side of the top electrode.

21. The capacitor of claim 20 wherein the top electrode couples to the electrode contacting line through a contact hole in the dielectric layer.

22. The capacitor of claim 21 wherein the contact hole comprises a plurality of separate holes.

23. The capacitor of claim 20, further comprising a second contact located on a top side of the bottom electrode.

24. The capacitor of claim 23, wherein the second contact extends away from the substrate farther than the second metal layer.

25. The capacitor of claim 20 wherein the bottom electrode and the electrode contacting line each have a planarized top surface.

26. The capacitor of claim 25 wherein the bottom electrode and the electrode contacting line are planarized by a damascene process.

27. The capacitor of claim 25 wherein the bottom electrode and the electrode contacting line are planarized by a CMP process performed on an interlayer dielectric layer.

28. The capacitor of claim 20 wherein the bottom electrode and the electrode contacting line are formed in a process other than planarization.

29. A method for forming a metal-insulator-metal capacitor in a semiconductor process, the method comprising:

forming an insulating layer on a semiconductor substrate;

forming a first connection wire and a second connection wire;

forming a bottom electrode on the insulating layer and disposed over the first connection wire;

forming a dielectric layer over the bottom electrode;

forming a top electrode disposed over the bottom electrode; and

forming a contact from the second connection wire to a bottom surface of the top electrode.

30. The method of claim 29, wherein forming the first and second connection wire comprises:

forming a first and a second trench in the insulating layer;

forming a metal layer within the first trench and the second trench; and

planarizing the metal layer to form a first connection wire in the first trench and a second connection wire in the second trench.

31. The method of claim 30, further comprising forming a barrier layer in the first and second trenches prior to forming the metal layer within the first and second trenches.

32. The method of claim 31 wherein forming a barrier layer comprises forming a layer from a material selected from a group consisting essentially of a transition metal, a transition metal alloy, a transition metal compound, and any combination thereof.

33. The method of claim 30 wherein forming the metal layer comprises forming a copper layer.

34. The method of claim 29, wherein forming the first and second connection wire comprises:

forming a conductive layer on the insulating layer;

patterning the conductive layer to form a first wire connection and a second wire connection;

depositing an interlayer dielectric layer on the first and second wire connections; and

planarizing the first and second wire connections and the interlayer dielectric layer.

35. The method of claim 34 wherein planarizing the first and second wire connections and the interlayer dielectric layer comprises performing a CMP process.

36. The method of claim 29, wherein forming the first and second connection wire comprises:

forming a conductive layer on the insulating layer; and

patterning the conductive layer to form a first wire connection and a second wire connection.

37. A method for forming a metal-insulator-metal capacitor in a semiconductor process, the method comprising:

forming an insulating layer on a semiconductor substrate;

forming a first wire connection and a second wire connection;

forming a first interlayer dielectric layer on the first wire connection and the second wire connection;

forming a first contact hole in the first interlayer dielectric layer to expose the first wire connection;

forming a bottom electrode on the first interlayer dielectric layer and within the first contact hole to contact the first wire connection;

forming a dielectric layer on the bottom electrode;

forming a second contact hole in the dielectric layer and in the first interlayer dielectric layer to contact the second wire connection; and

forming a top electrode disposed over the bottom electrode and within the second contact hole to contact the second wire connection.

38. The method of claim 37, wherein forming the first and second wire connection comprises:

forming a first and a second trench in the insulating layer;

forming a conductive layer within the first trench and the second trench; and

planarizing the conductive layer to form a first wire connection in the first trench and a second wire connection in the second trench.

39. The method of claim 37, wherein forming the first and second connection wire comprises:

forming a conductive layer on the insulating layer;

patterning the conductive layer to form a first wire connection and a second wire connection;

depositing an interlayer dielectric layer on the first and second wire connections; and

planarizing the first and second wire connections and the interlayer dielectric layer.

40. The method of claim 37, wherein forming the first and second wire connection comprises:

forming a conductive layer on the insulating layer; and

patterning the conductive layer to form a first wire connection and a second wire connection.

41. The method of claim 37 wherein forming the first contact hole comprises forming a plurality of separate contact holes.

42. The method of claim 37 wherein forming the second contact hole comprises forming a second plurality of separate contact holes.

43. A method for forming a metal-insulator-metal capacitor in a semiconductor process, the method comprising:

forming an insulating layer on a semiconductor substrate;

forming a first wire connection and a bottom electrode;

forming a dielectric layer on the first wire connection and the bottom electrode;

forming a first contact hole in the dielectric layer and disposed over the first wire connection;

forming a top electrode disposed over the dielectric layer and within the first contact hole to contact the first wire connection;

forming a interlayer dielectric layer disposed over the top electrode, the dielectric layer, and the bottom electrode;

forming a second contact hole in the interlayer dielectric layer and in the dielectric layer to expose the bottom electrode; and

forming a contact plug within the second contact hole and structured to contact a top surface of the bottom electrode.

44. The method of claim 43, wherein forming the first wire connection and the bottom electrode comprises:

forming a first and a second trench in the insulating layer;

forming a conductive layer within the first trench and the second trench; and

planarizing the conductive layer to form a first wire connection in the first trench and a bottom electrode in the second trench.

45. The method of claim 43, wherein forming the first wire connection and the bottom electrode comprises:

forming a conductive layer on the insulating layer;

patterning the conductive layer to form a first wire connection and a bottom electrode;

depositing an interlayer dielectric layer on the first wire connection and the bottom electrode; and

planarizing the first wire connection, the bottom electrode, and the interlayer dielectric layer.

46. The method of claim 43, wherein forming the first wire connection and the bottom electrode comprises:

forming a conductive layer on the insulating layer; and

patterning the conductive layer to form a first wire connection and a bottom electrode.

47. A method for forming a metal-insulator-metal capacitor in a semiconductor process and on a semiconductor substrate having an insulating layer formed thereon, the method comprising:

forming a connection line on the insulating layer;

forming a bottom electrode on the insulating layer;

forming a capacitor dielectric layer disposed on the bottom electrode;

forming a top electrode disposed on the capacitor dielectric layer; and

coupling the connection line to a bottom surface of the top electrode.

48. The method of claim 47 wherein forming the connection line comprises:

forming a first and second trench in the insulating layer;

forming a barrier layer in the first and second trench;

forming a metal layer on the barrier layer; and

planarizing the metal layer.

49. The method of claim 48 wherein forming a metal layer comprises electroplating the barrier layer.

50. The method of claim 48 wherein forming a barrier layer comprises forming a layer including titanium.

51. The method of claim 47 wherein forming the connection line comprises:

forming a metal layer on the insulating layer;

patterning the metal layer to form a connection line;

forming a second insulating layer on the connection line; and

planarizing the metal layer and the second insulating layer by chemical-mechanical-polishing.